## AMENDMENTS TO THE SPECIFICATION

On page 6, amend the paragraph beginning at line 17 as follows:

Figure 3[[,]] shows the resulting electrical circuit for the relevant portion 300 of the memory array when row 280 is grounded. As shown, memory element 310 to be sensed is connected between a grounded row line 280 and a particular column line 320. Also connected to the column line 320 ~~are~~ is a plurality of other resistive memory elements (e.g., elements 330, 340, 350, 360, 370) each of which is connected at its opposite end to a pull-up voltage source $V_A$ 215 through a respective row line 210. In addition, a respective sensing circuit 400 is connected to the column line 320. The sensing circuit 400 includes a voltage supply that maintains the column line 320 at electrical potential $V_A$.

On page 8 amend the paragraph beginning at line 12 as follows

The resistance measuring circuit 500 outputs a bit stream from an output 900 of a comparator 910. The ratio of logic one bits to a total number of bits (or, in ~~and other~~ another aspect of the invention, the ratio of logic one bits to logic zero bits) in the bit stream yields a numerical value. This numerical value corresponds to the current that flows through the resistance 520 in response to a known applied voltage. For example, assume that a current source can deliver current at two discrete current levels, corresponding to two different states of a logical input signal. When the signal is in logic one state, the source delivers, for example, 2 μA. When the signal is in a logic zero state, the source delivers, for example, 0 μA. The logical input signal is monitored over a finite time span corresponding to a number of bit-length time periods. Over that time span, the ~~number~~ numbers of logic one and logic zero bits are recorded. By

straightforward algebra, the average current delivered by the current source over the corresponding time span may be calculated as follows:

$$IAVG = \frac{(\text{number of logic 1 bits})*2\mu A + (\text{number of logic 0 bits})*0\mu A}{\text{total number of bits in the signal}}$$

As an example, if, over a time span corresponding to 4 cycles, there is one logic one bit and three logic zero bits then the average current over the four cycles is 0.5μA.

$$IAVG = \frac{1*2\mu A + 3*0\mu A}{4} = 0.5\ \mu A$$

On page 14, amend the paragraph beginning at line 3 as follows:

Figure 7 ~~9~~ shows a computer system 1200 including a digital memory 1210 having a resistance measuring memory cell sensor according to the invention. The computer 1200, as shown includes a central processing unit (CPU) 1220, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 1230 over a bus 1240. The computer system also includes peripheral devices such as disk storage 1250 and a user interface 1260. It may be desirable to integrate the processor and memory on a single IC chip.